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00862.023385.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Nobushige KORENAGA

Application No.: 10/735,650 }

Filed: December 16, 2003

For: ALIGNMENT APPARATUS AND EXPOSURE
APPARATUS USING THE SAME

)
: Examiner: J. Waks
)
: Group Art Unit: 2834
)
: Confirmation No.: 3534
)
: Allowed: August 1, 2005
)
: August 17, 2005

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

LETTER REQUESTING CONSIDERATION
OF PAPERS TIMELY FILED

Sir:

Applicant has received a Notice of Allowance and a Notice of Allowability dated August 1, 2005, in the above-identified application. However, in reviewing the Notice of Allowability, Applicant notes that the Examiner has not yet acknowledged receipt of the Submission of Priority Documents and the certified copies of the priority documents that were filed in the U.S. Patent and Trademark Office on February 12, 2004, submitting the certified copies of Japanese patent document numbers 2002-382495, filed December 27, 2002, and 2003-123832, filed April 28, 2003. For the Examiner's convenience, attached are copies of (1) the Submission of Priority Documents, (2) the cover page and drawings of the priority documents

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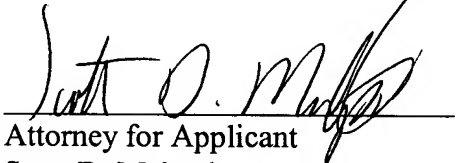
(the only portions retained) and (3) the date stamped post card receipt indicating that these papers were received by the U.S. Patent and Trademark Office on February 12, 2004.

Applicant requests that the Examiner acknowledge receipt of the certified copies of the priority documents.

Applicant believes that no fees should be incurred in connection with filing this paper. However, the Commissioner is authorized to charge Deposit Account No. 06-1205, should any fees be associated herewith.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should be directed to our address listed below.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Scott D. Malpede", is written over a horizontal line.

Attorney for Applicant
Scott D. Malpede
Registration No. 32,533

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
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Date 2 / 12 / 2004
Mo. Day Yr.
Atty. Docket 00862-023385
Application 16735650

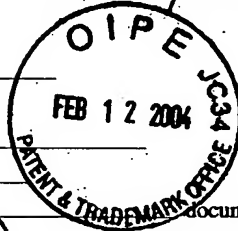
Sir:
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- ☐ Notice of Appeal and Check for \$ _____
- ☐ Information Disclosure Statement, PTO-1449 and _____ documents
- ☒ Claim for priority and certified copies of two (2) priority applications
- ☐ Issue fee transmittal and Check for \$ _____
- ☐ Other (specify) _____

by placing your receiving date stamp hereon and returning to deliverer.

Atty. SEW/EDS

Due Date _____
Mo. Day Yr.



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APPARATUS USING THE SAME

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: Examiner: Unassigned
)
: Group Art Unit: Unassigned
)
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)
:
) February 12, 2004
:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF PRIORITY DOCUMENTS

Sir:

In support of Applicant's claim for priority under 35 U.S.C. § 119, enclosed are two certified copies of the following foreign applications:

JAPAN 2002-382495, filed December 27, 2002; and

JAPAN 2003-123832, filed April 28, 2003.

Applicant's undersigned attorney may be reached in our Washington, D.C., office by telephone at (202) 530-1010. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

Attorney for Applicant
Steven E. Warner
Registration No. 33,326

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30 Rockefeller Plaza
New York, New York 10112-3801
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SEW/eab

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日本国特許庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 2002年12月27日
Date of Application:

出願番号 特願2002-382495
Application Number:
[JP2002-382495]
ST. 10/C]:

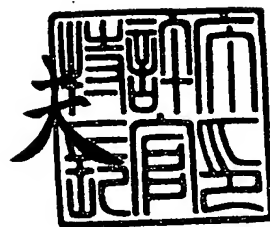
願人 キヤノン株式会社
Applicant(s):

CERTIFIED COPY OF
PRIORITY DOCUMENT

2004年 1月14日

特許庁長官
Commissioner,
Japan Patent Office

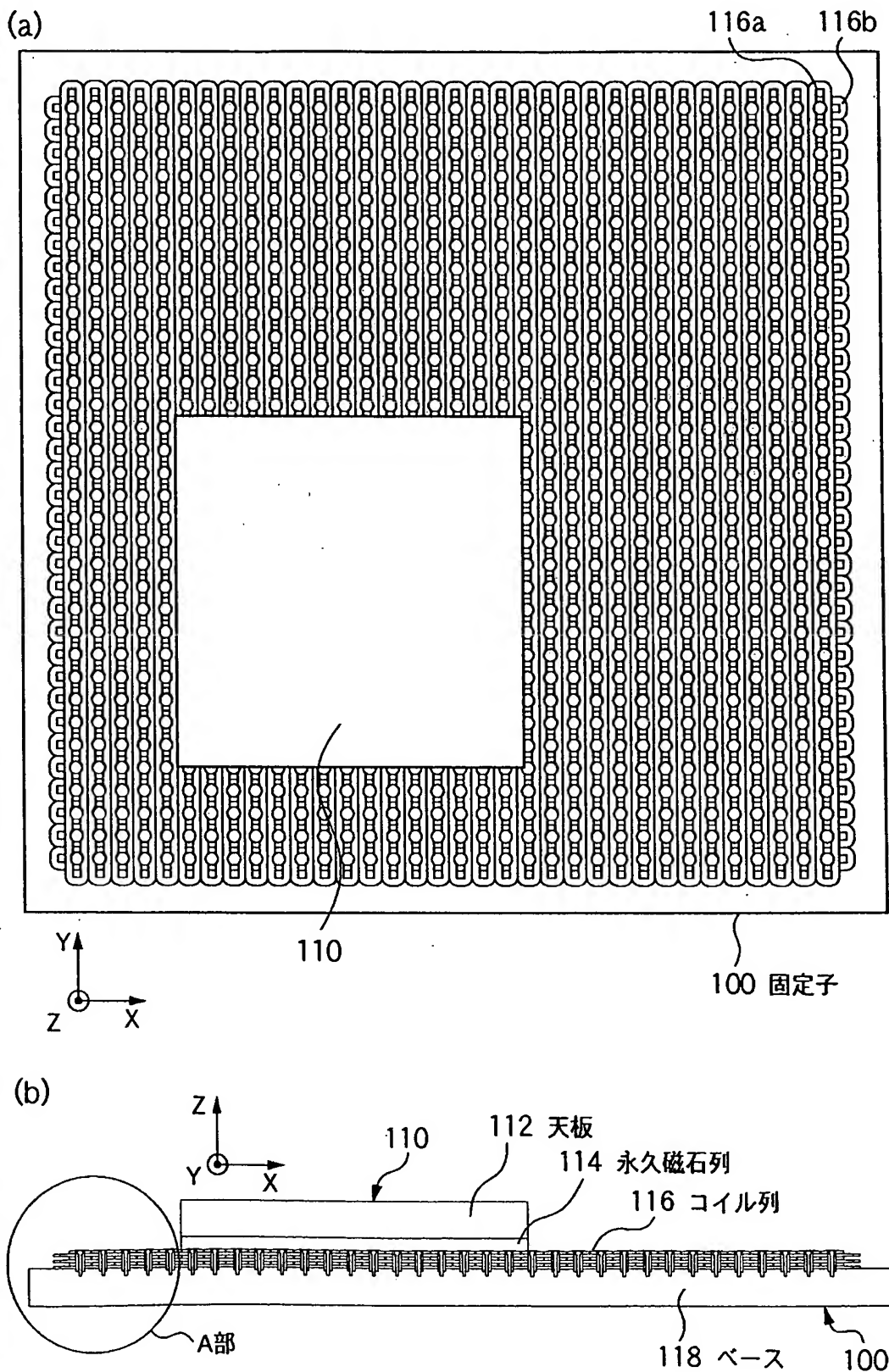
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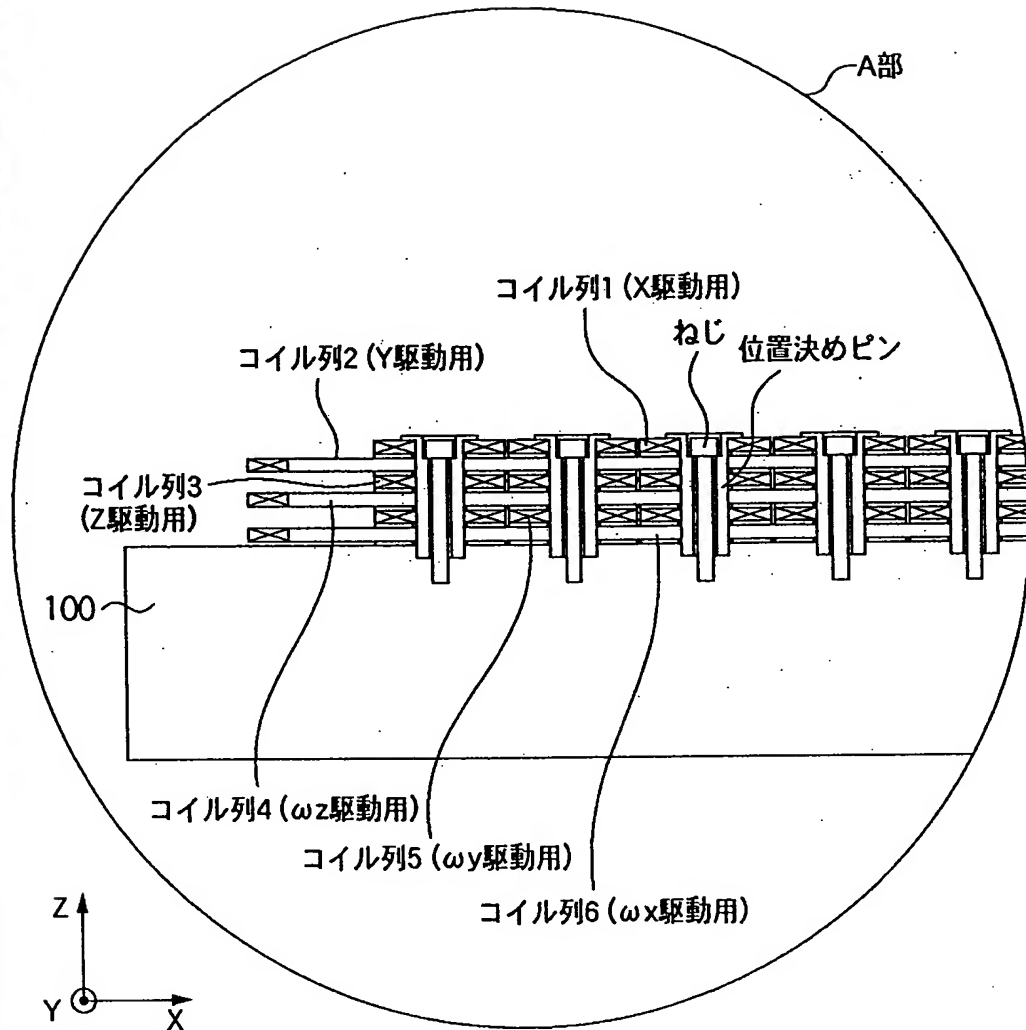
【書類名】

図面

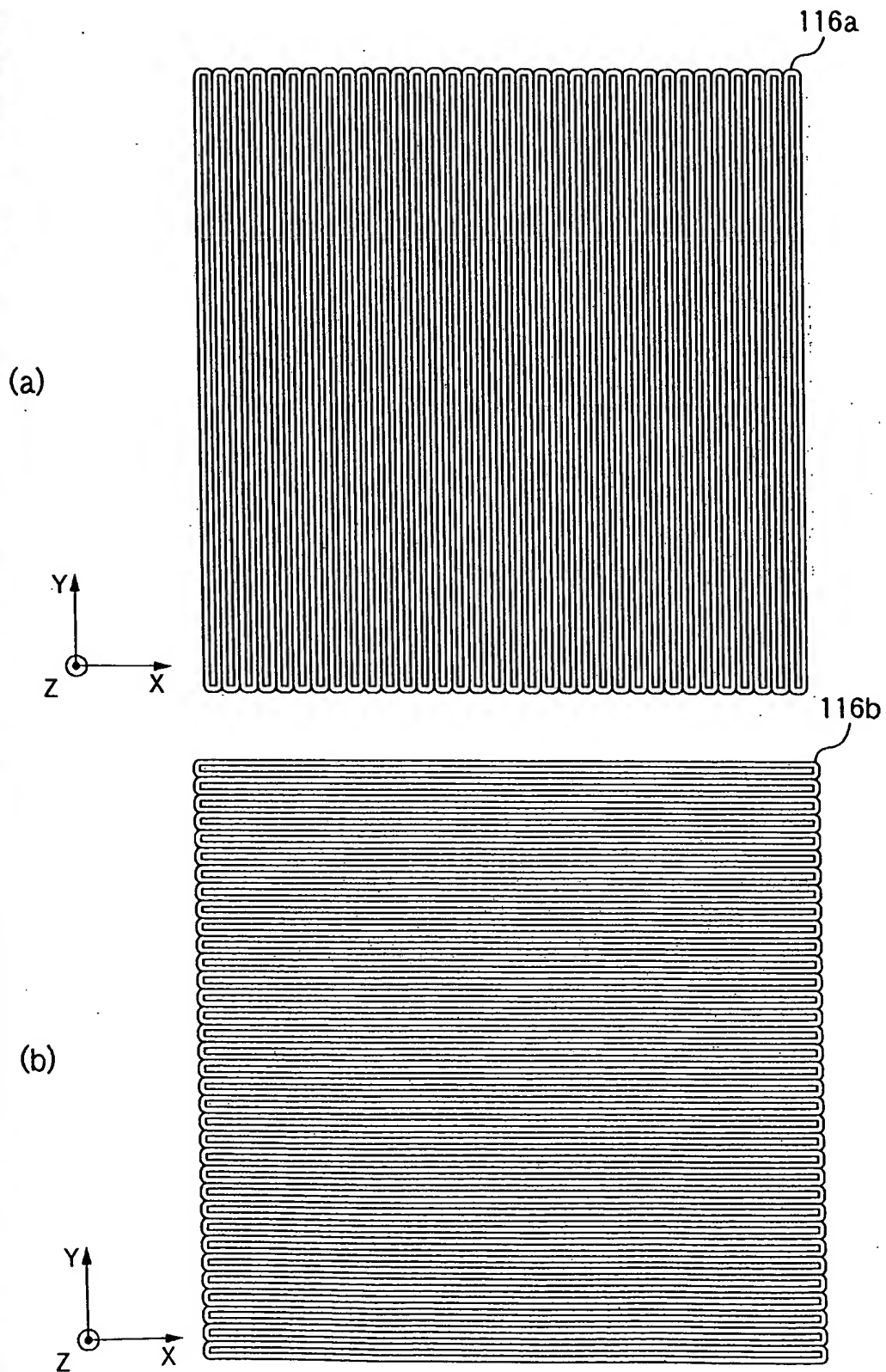
【図 1】



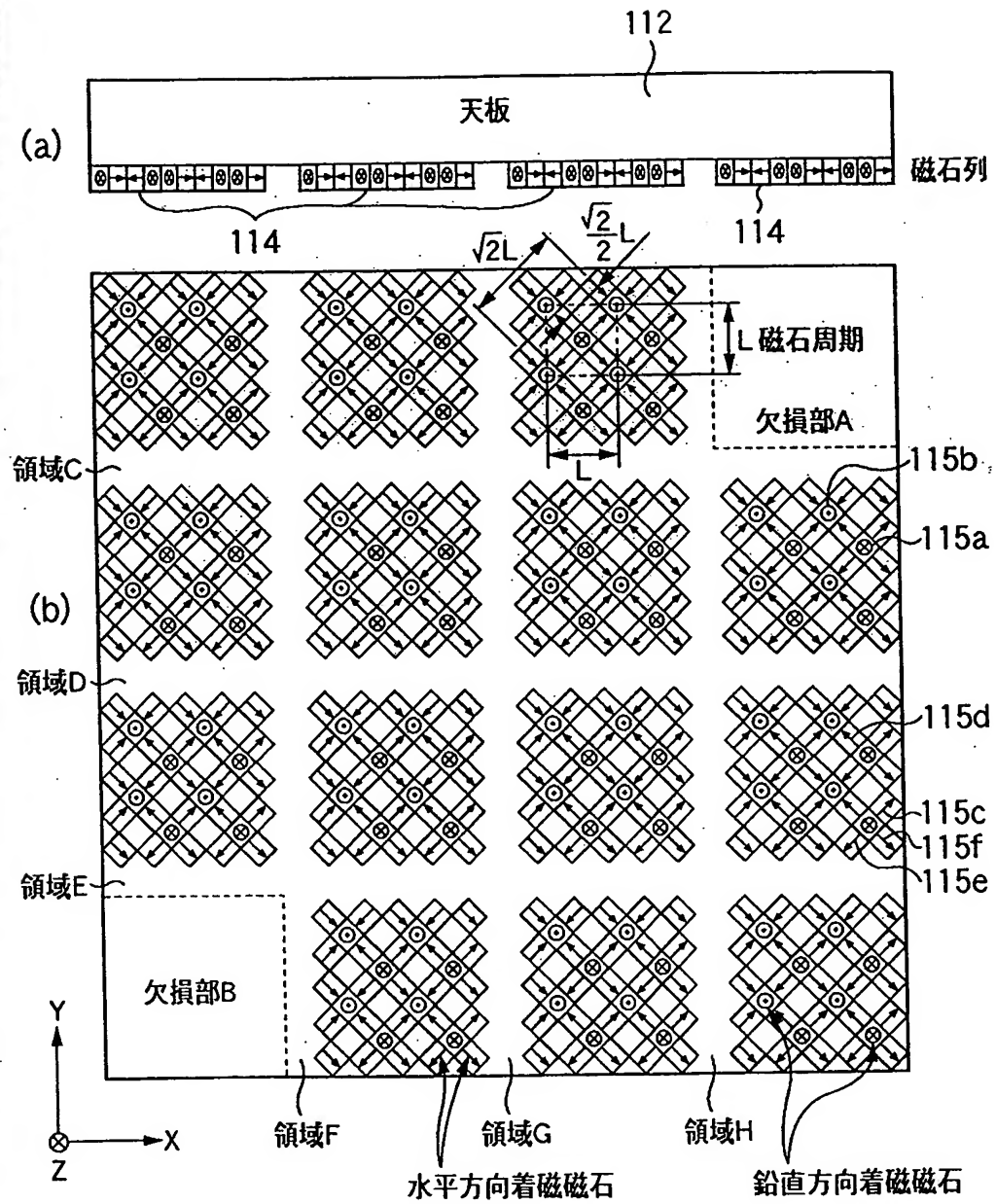
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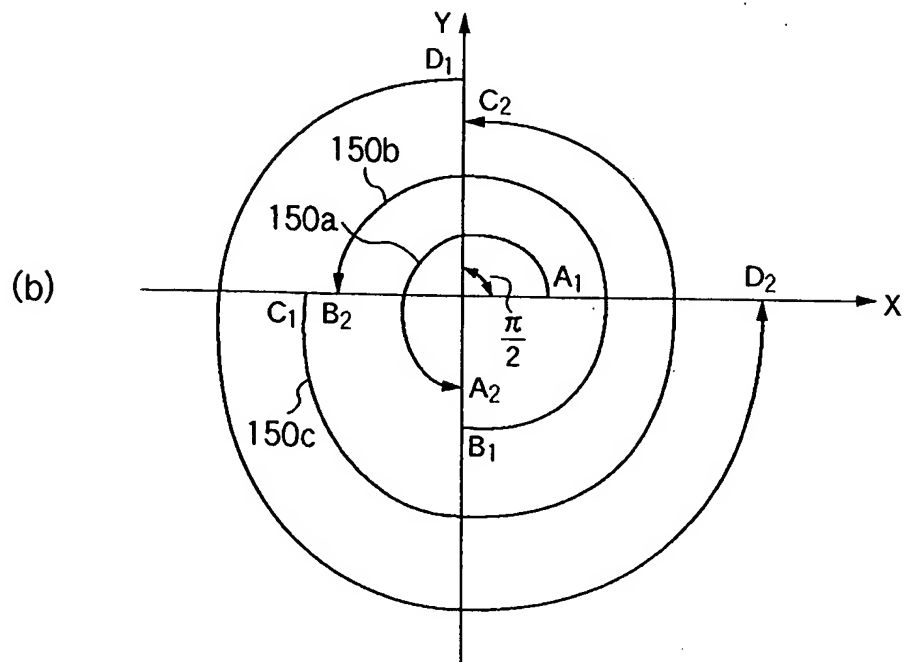
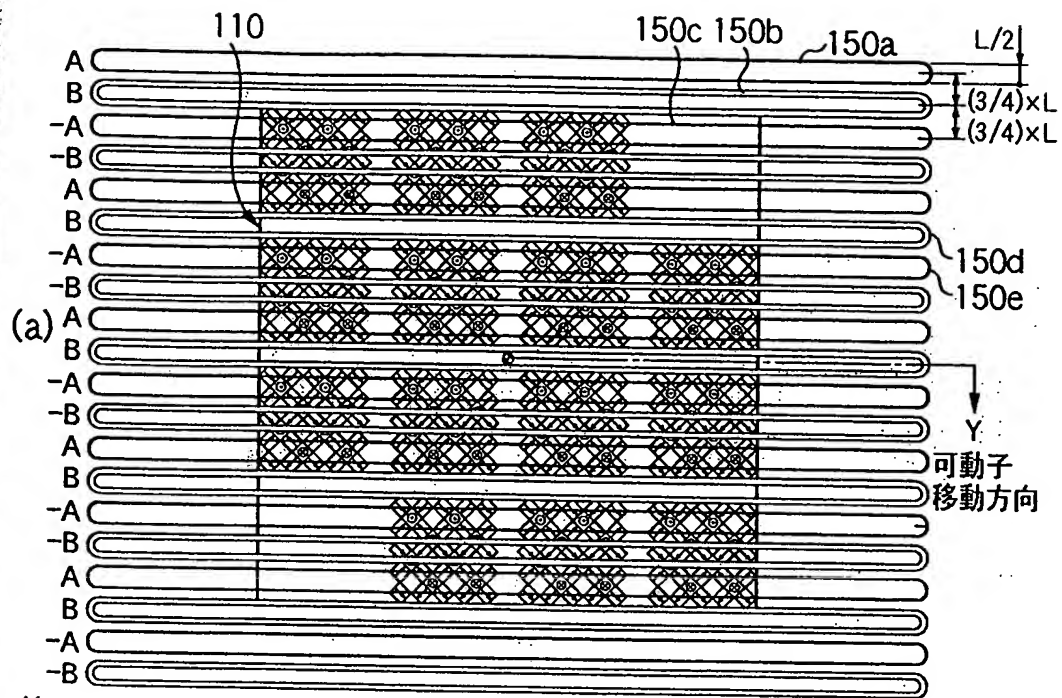
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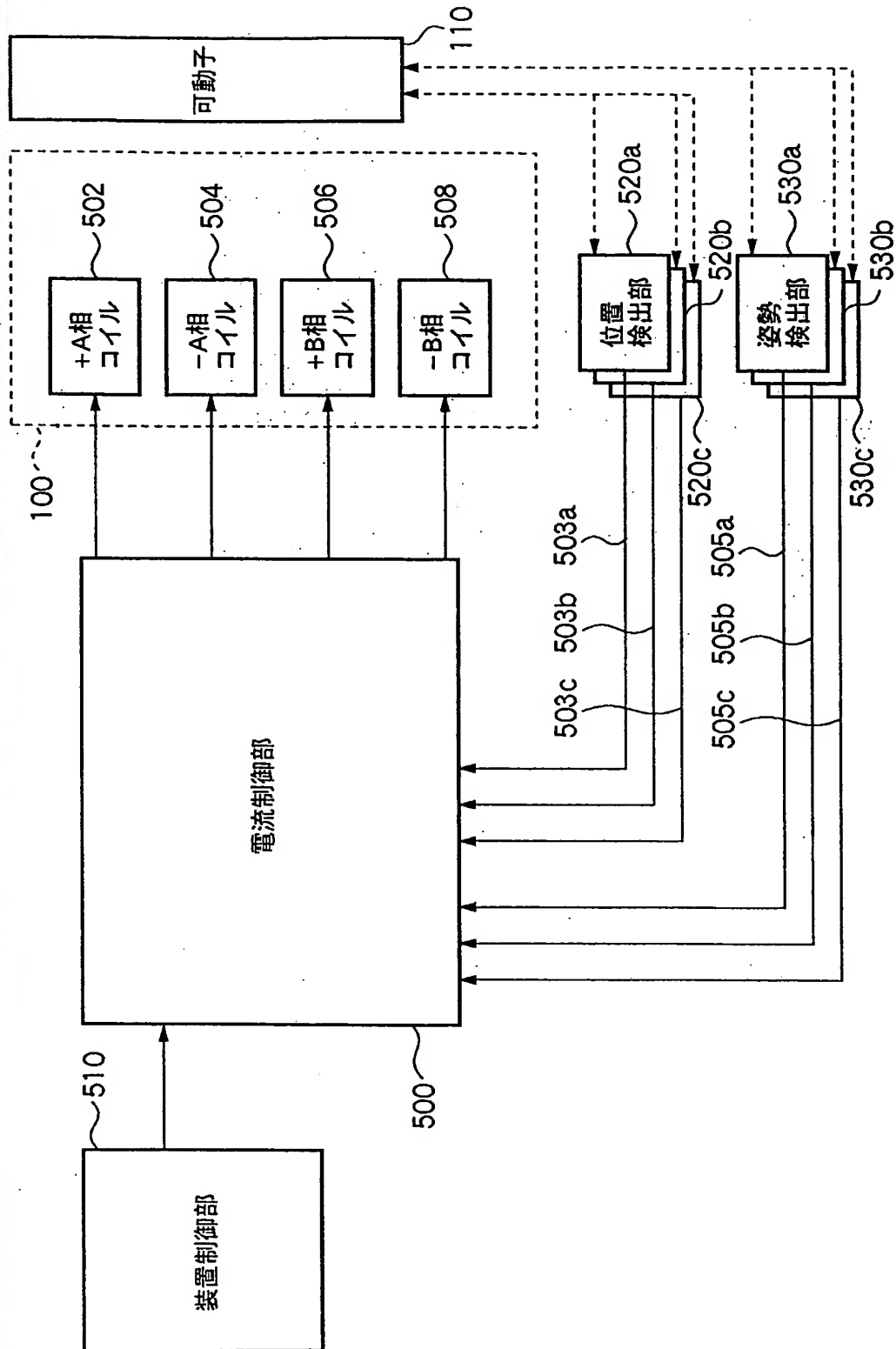
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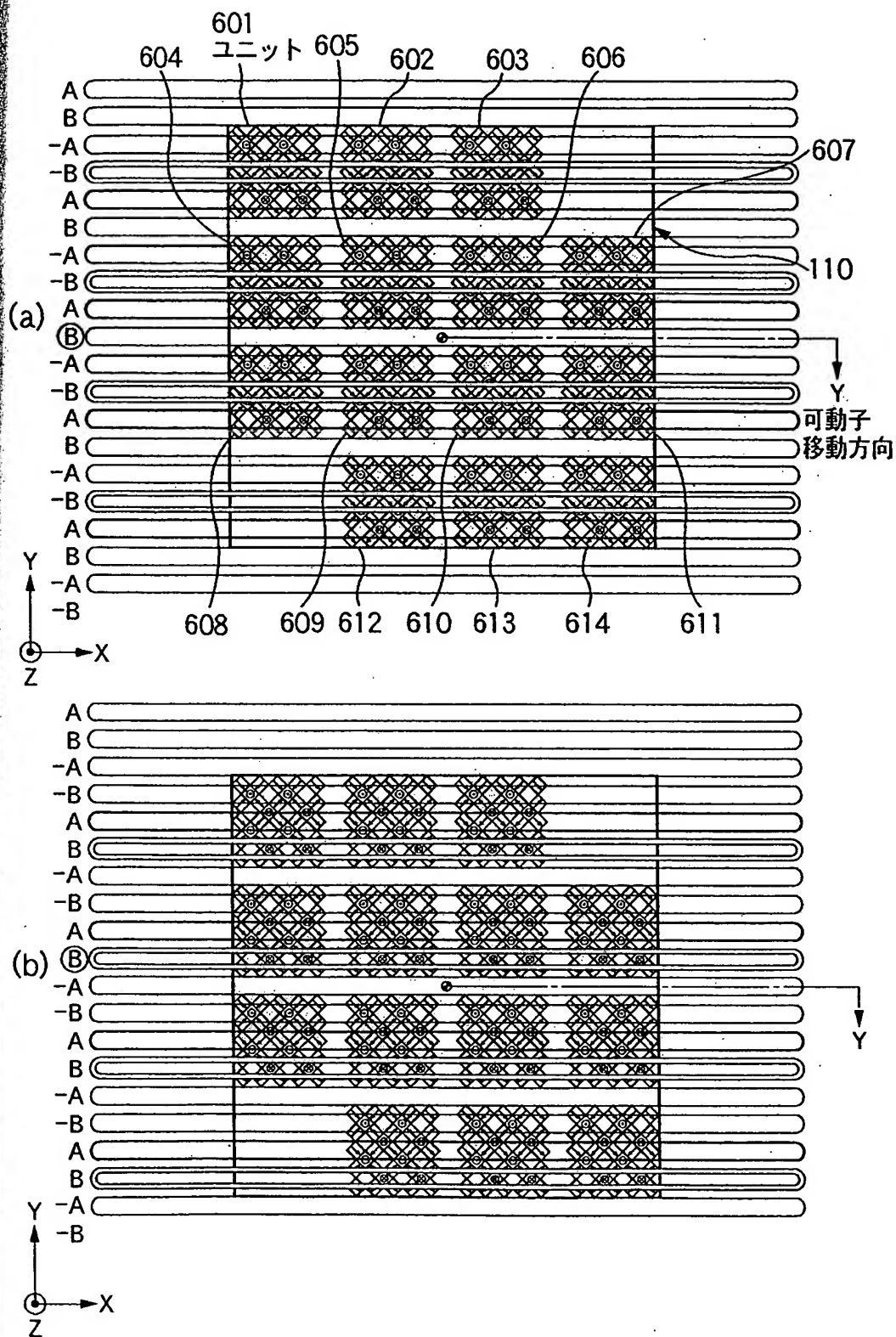
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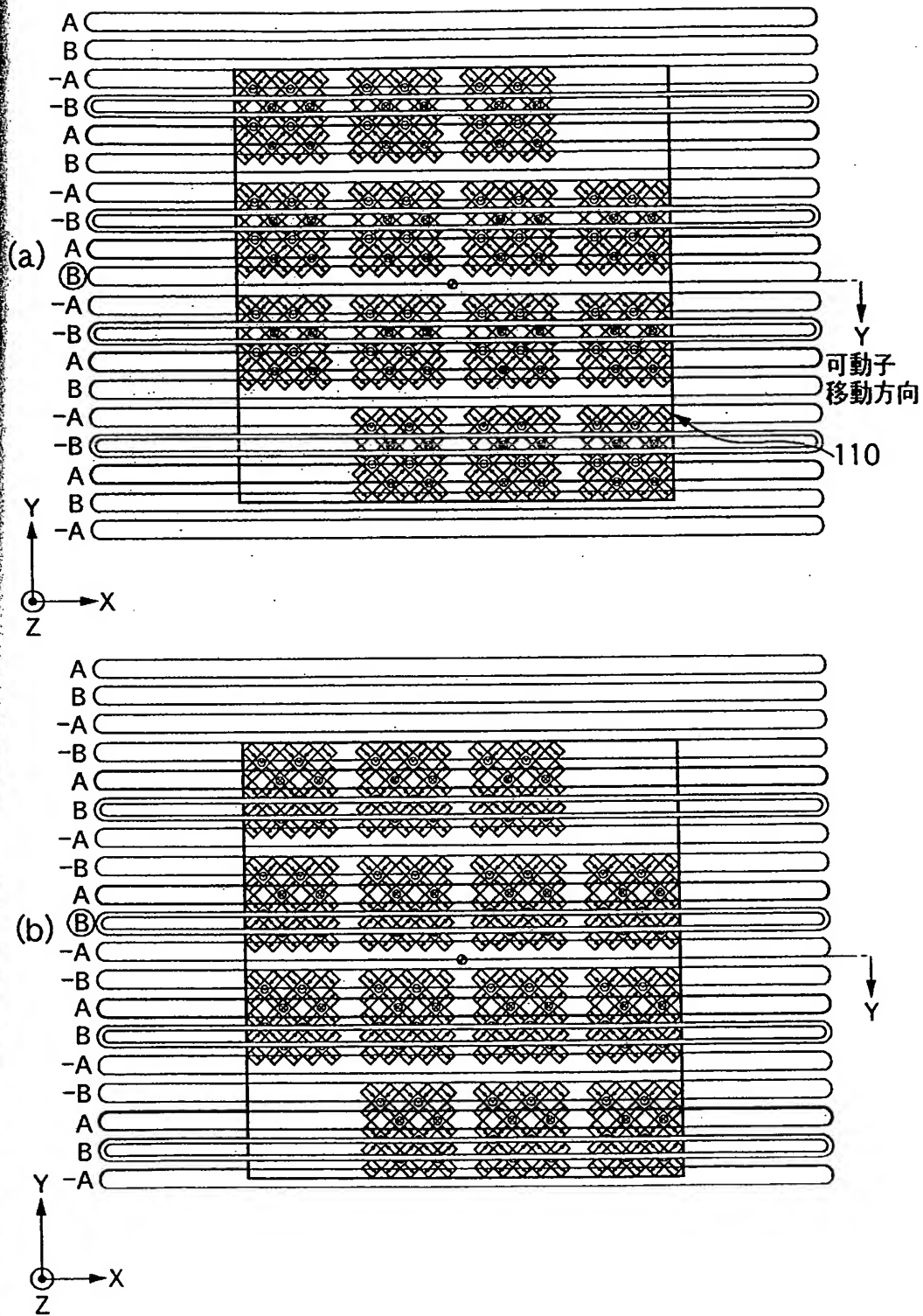
【図 5 B】



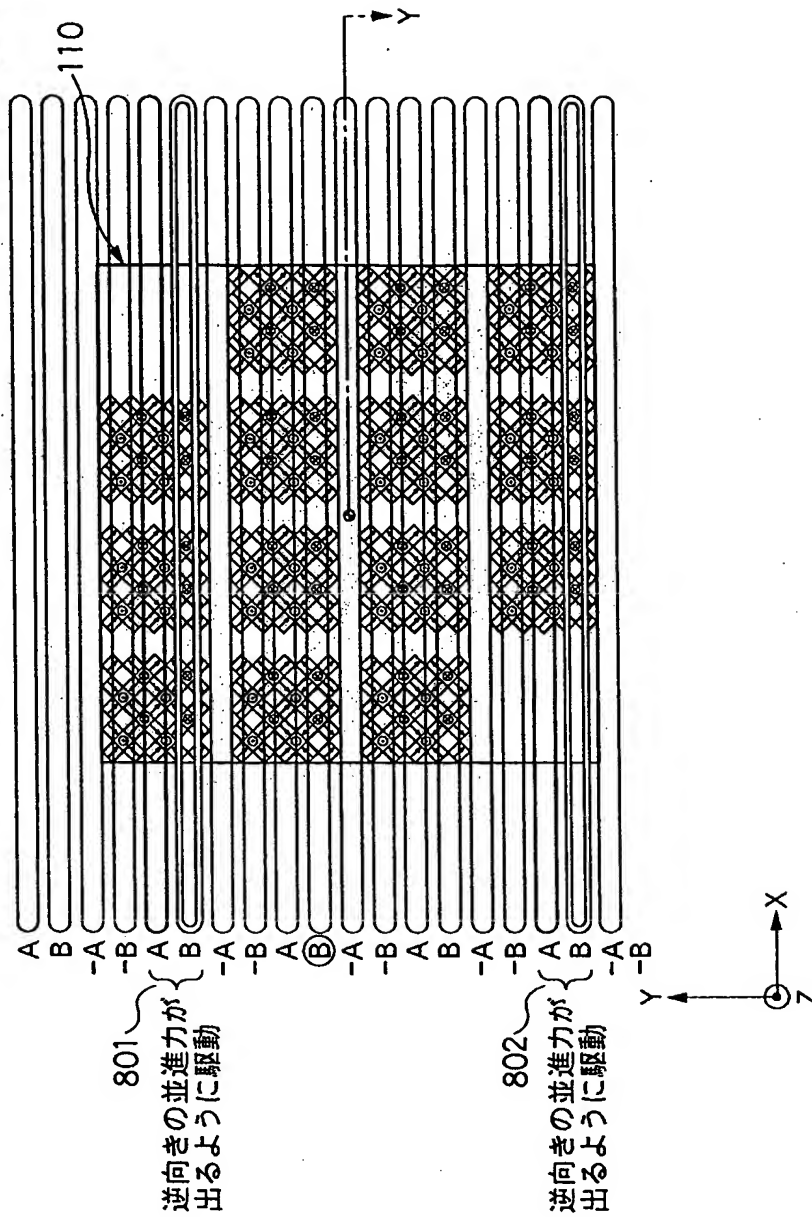
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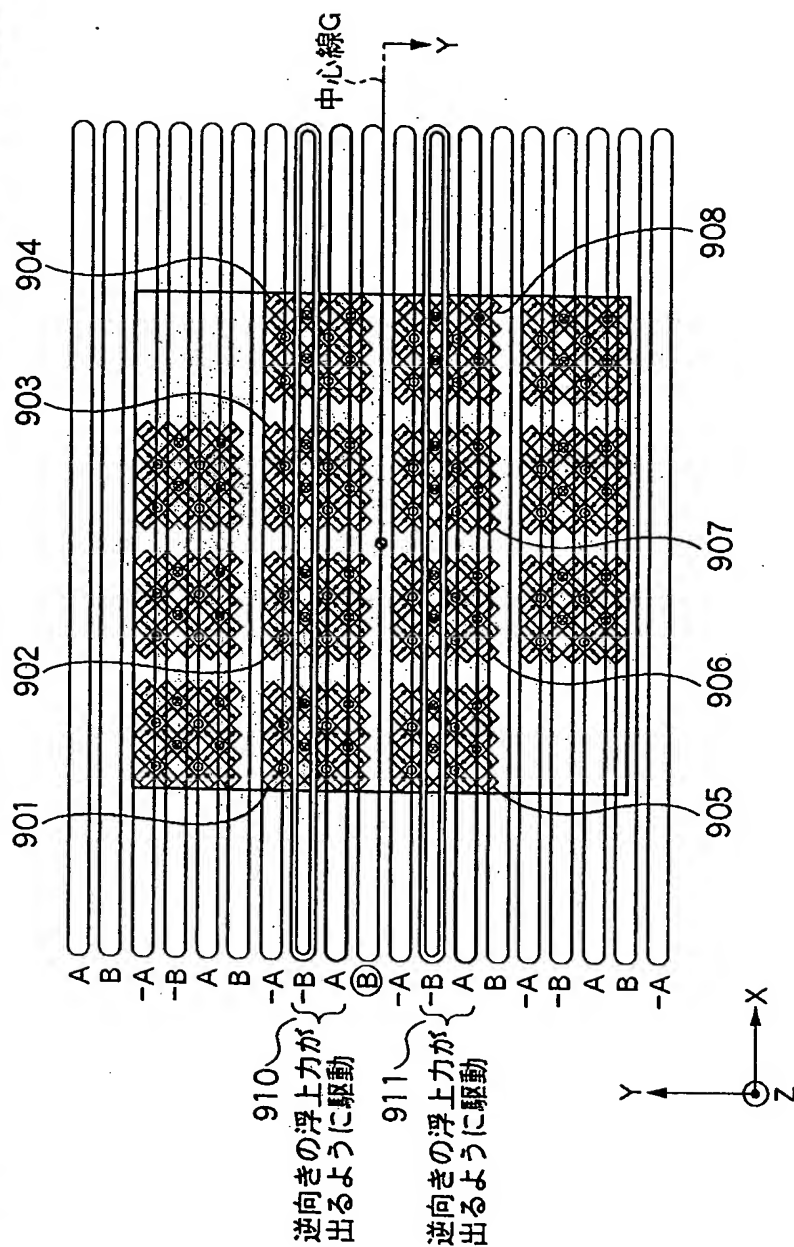
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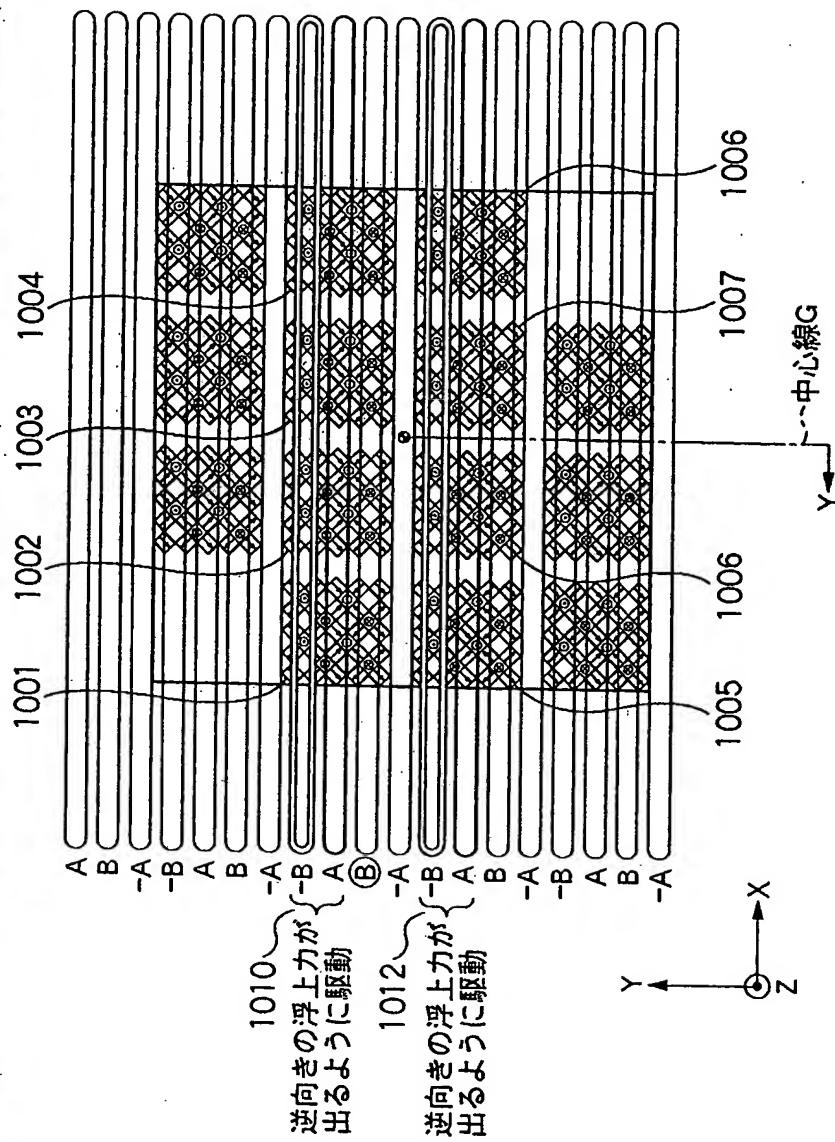
【图 8】



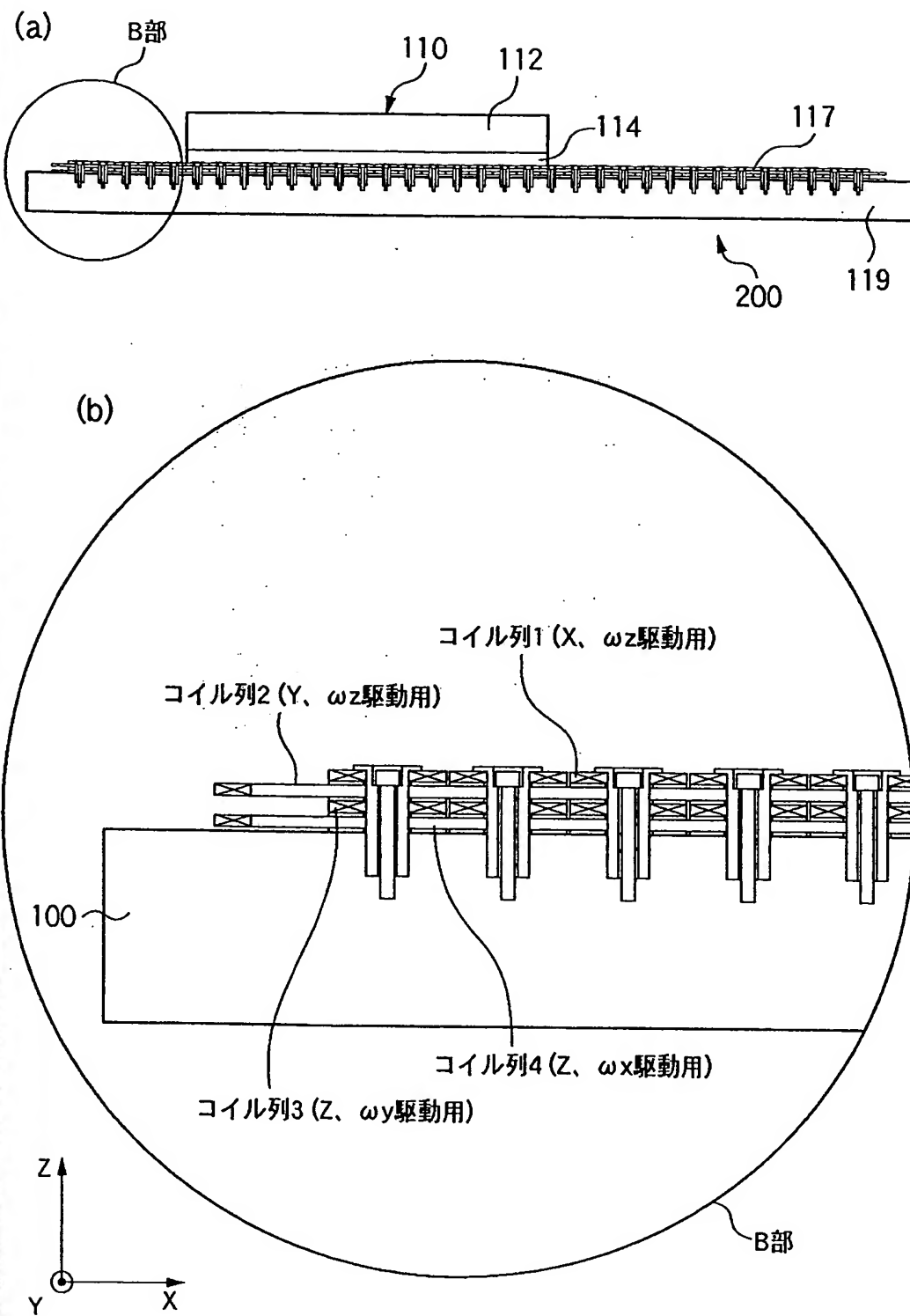
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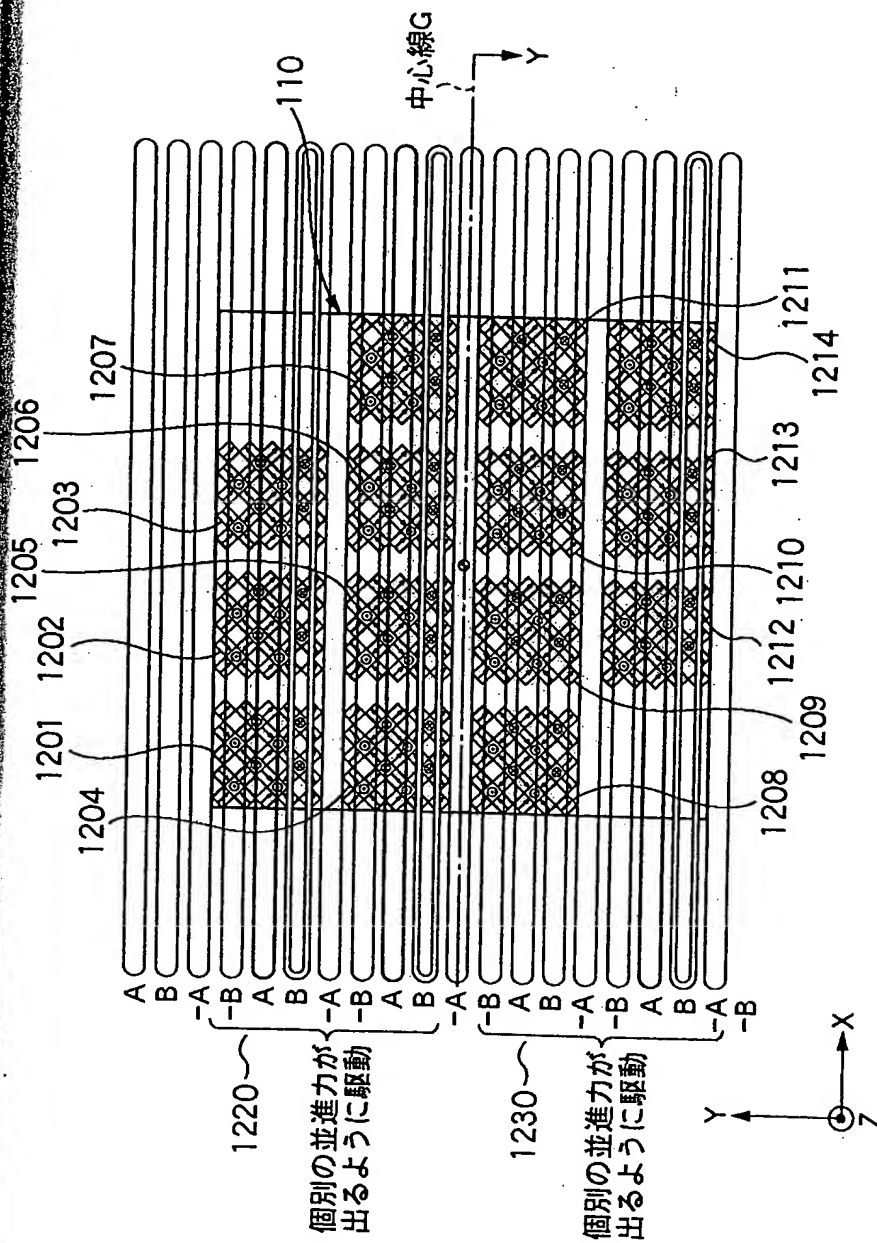
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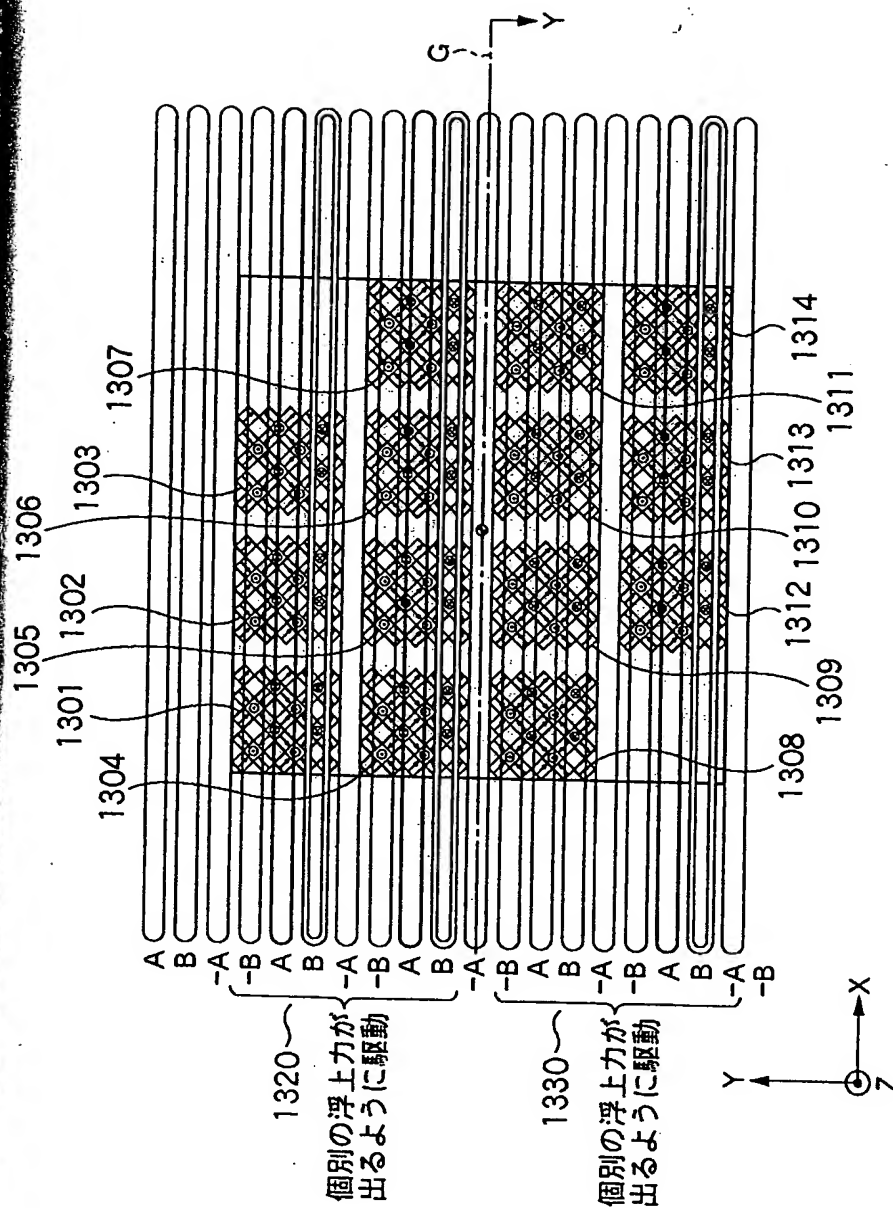
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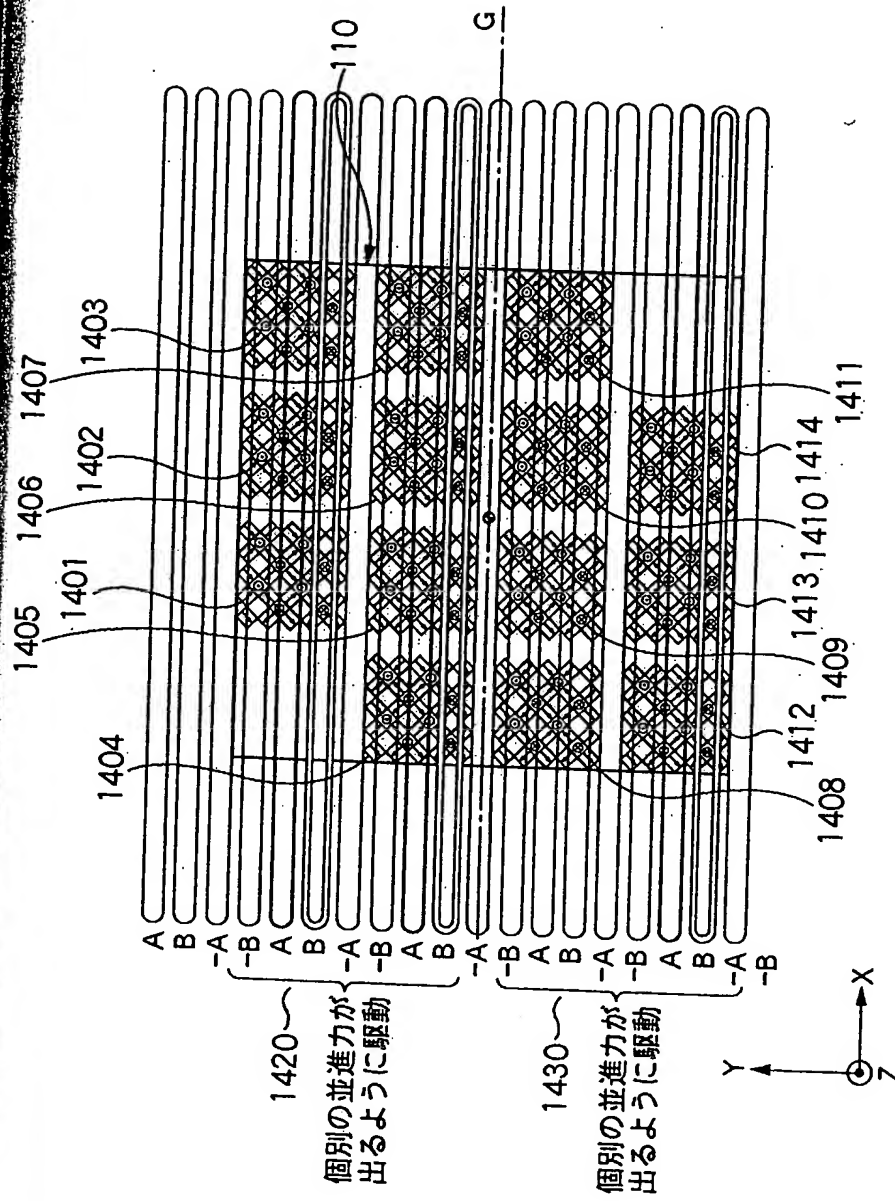
【図 12】



【図13】



【図 14】



【図 15】

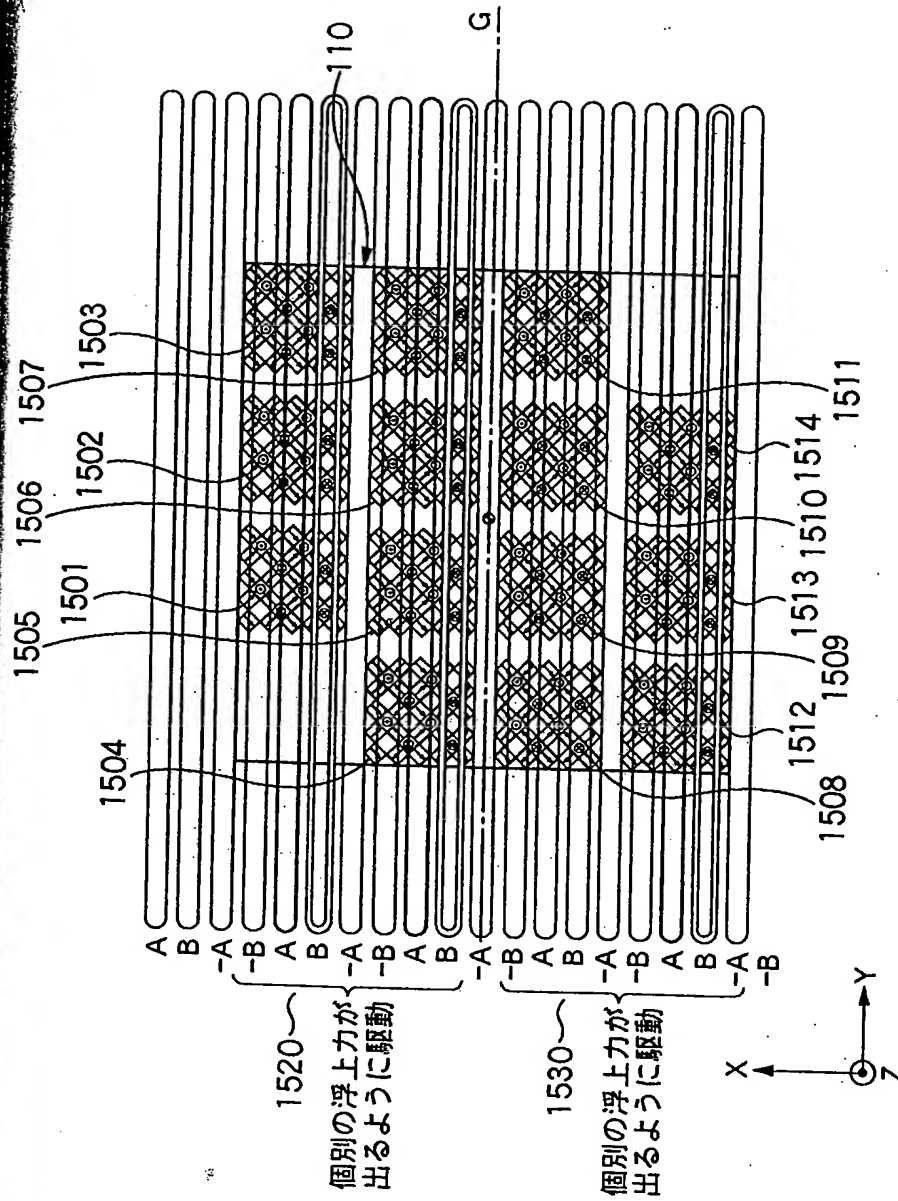
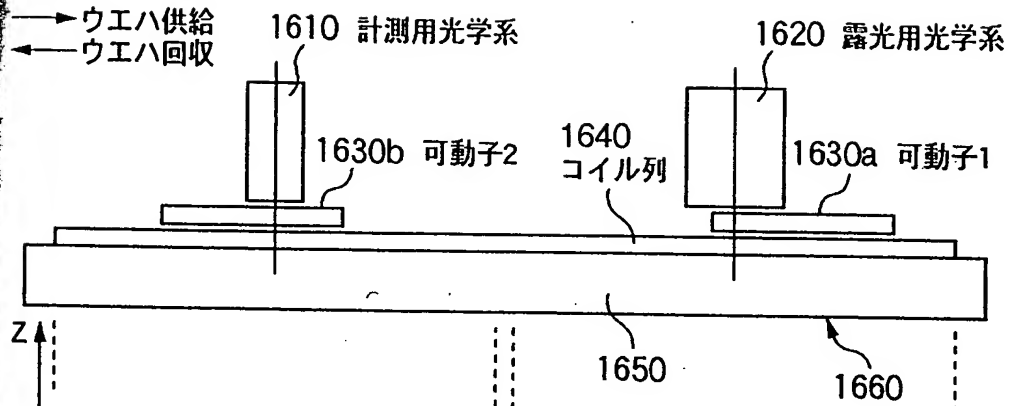
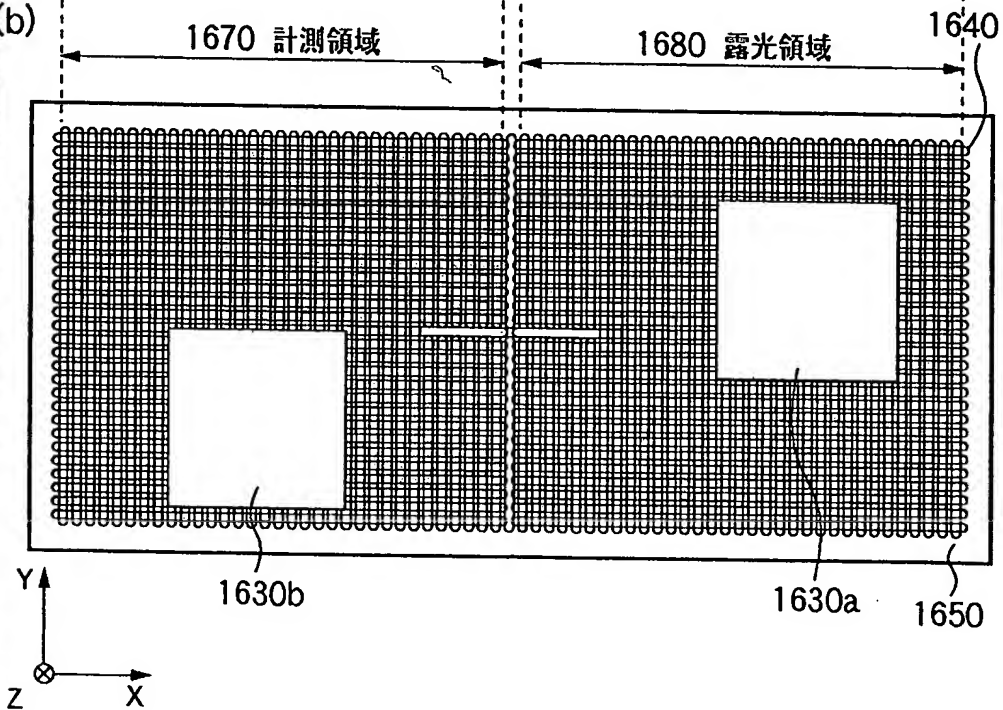


図 16 A]

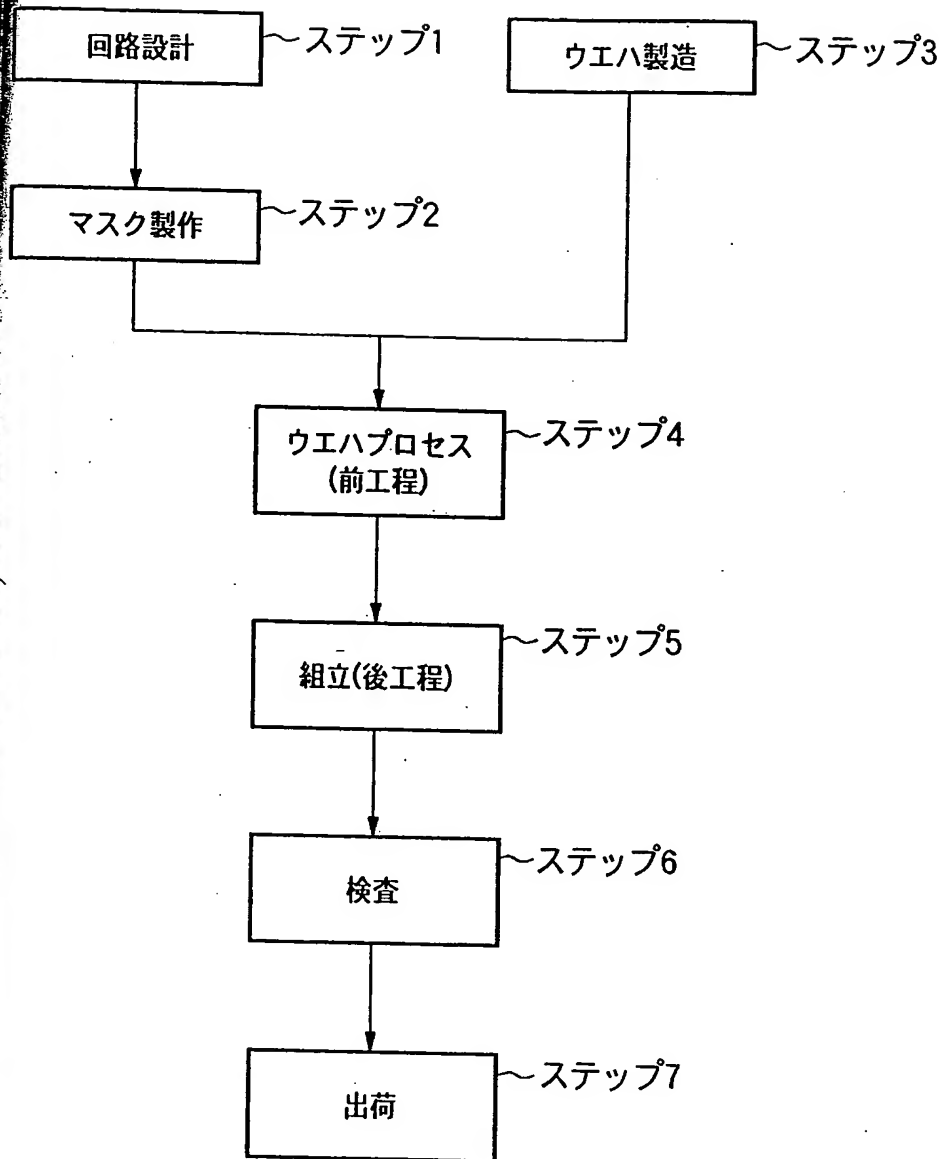
(a)



(b)



【図16B】



半導体デバイス製造フロー

【図 17】

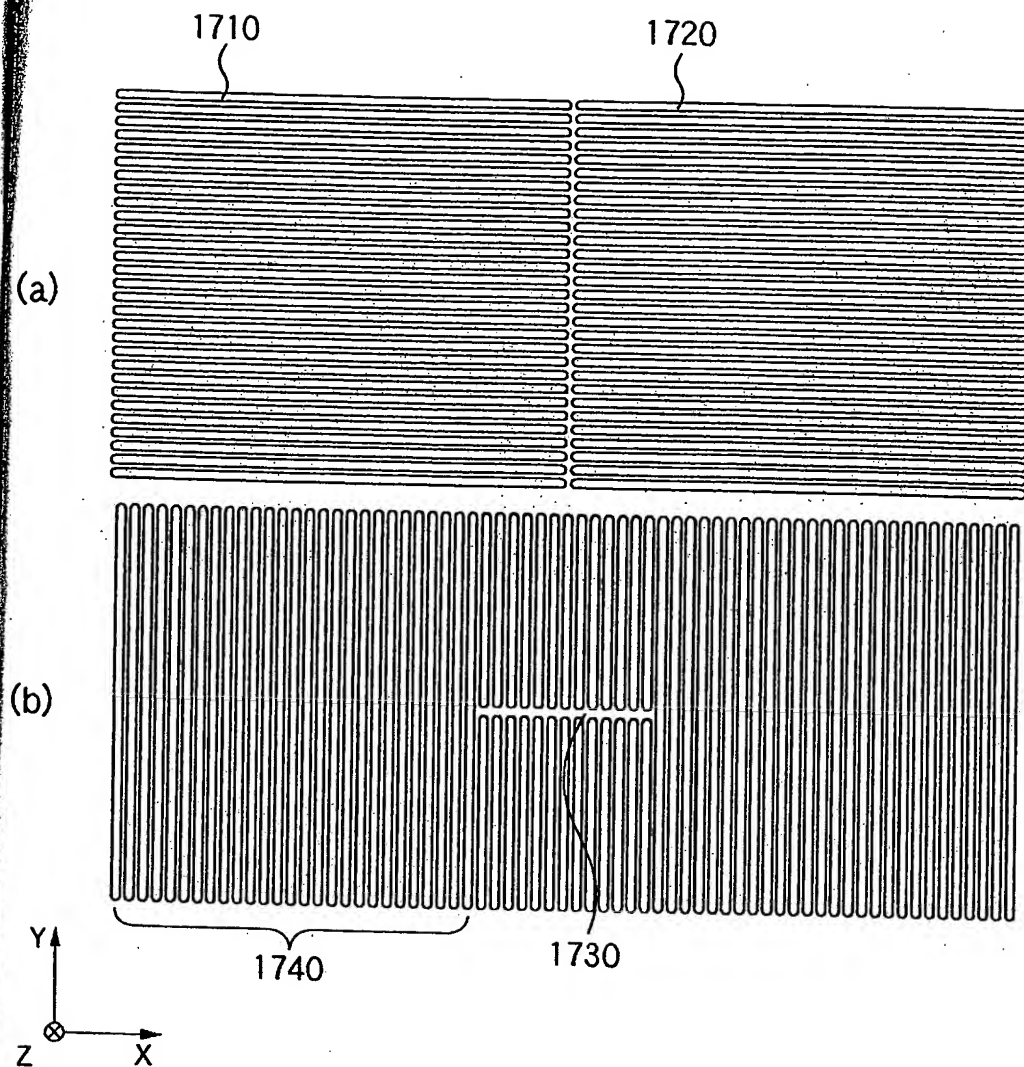
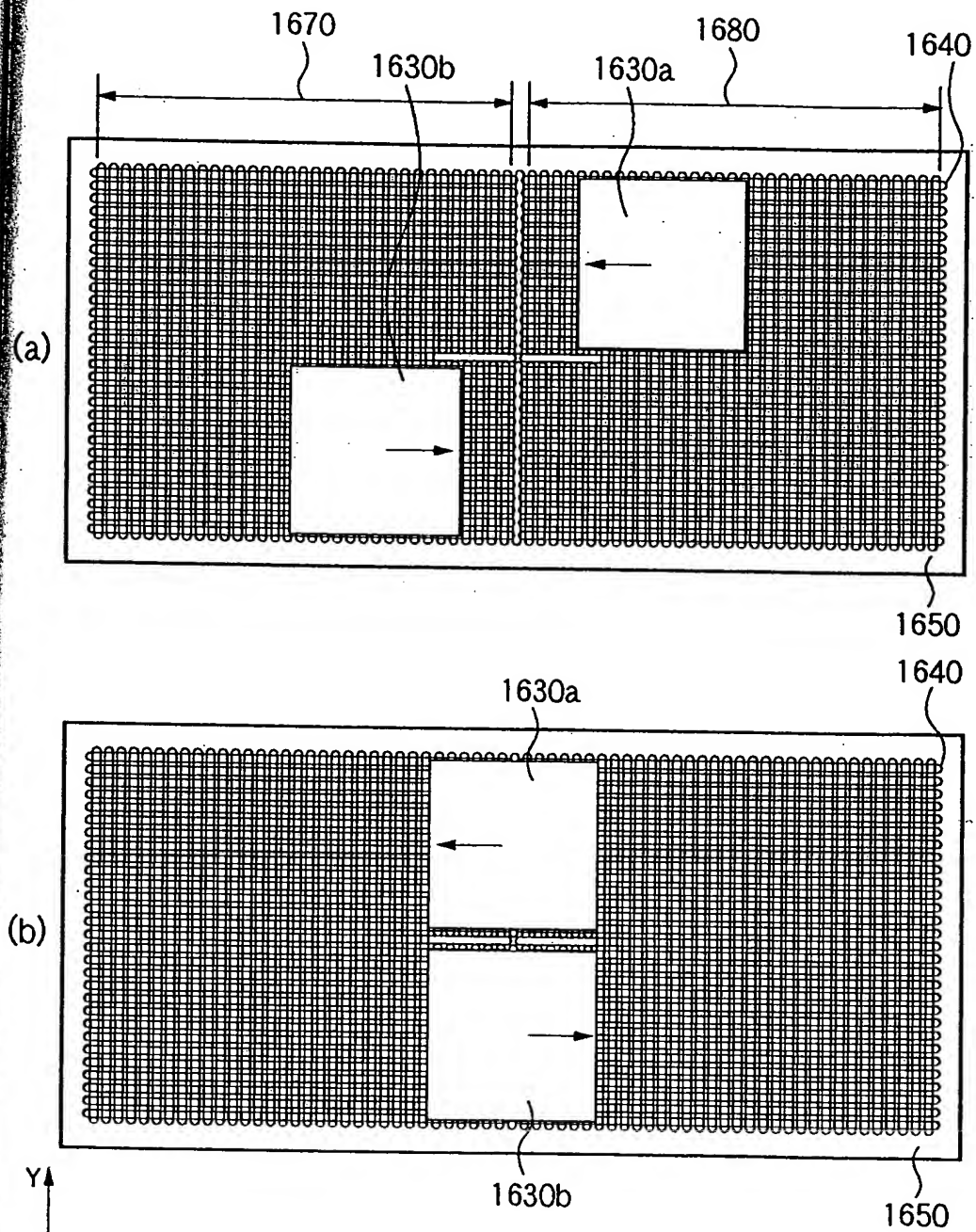
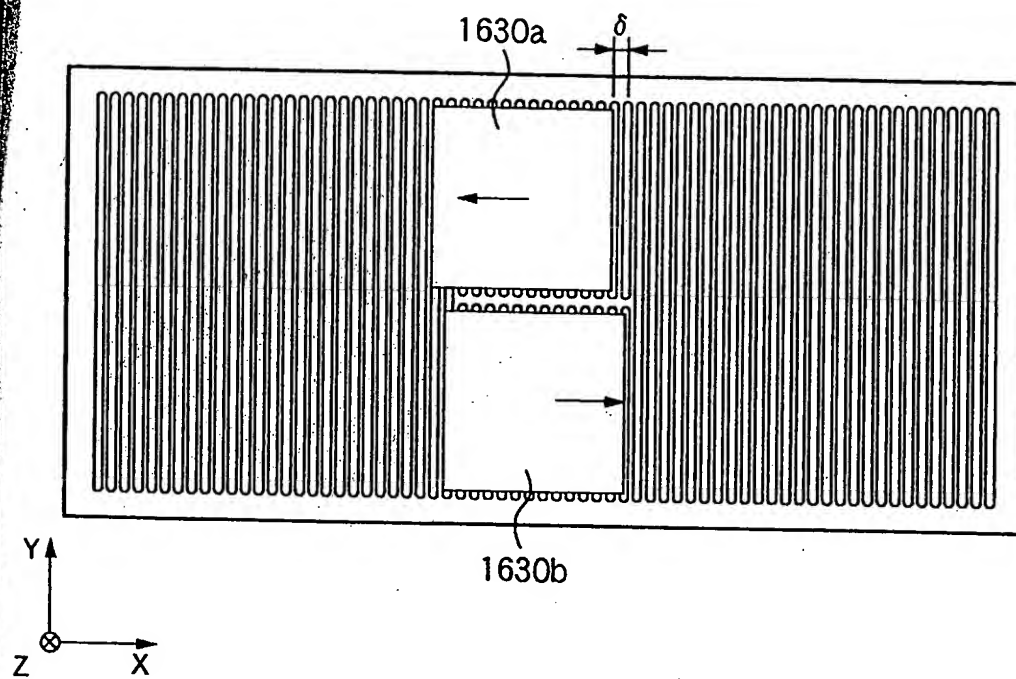


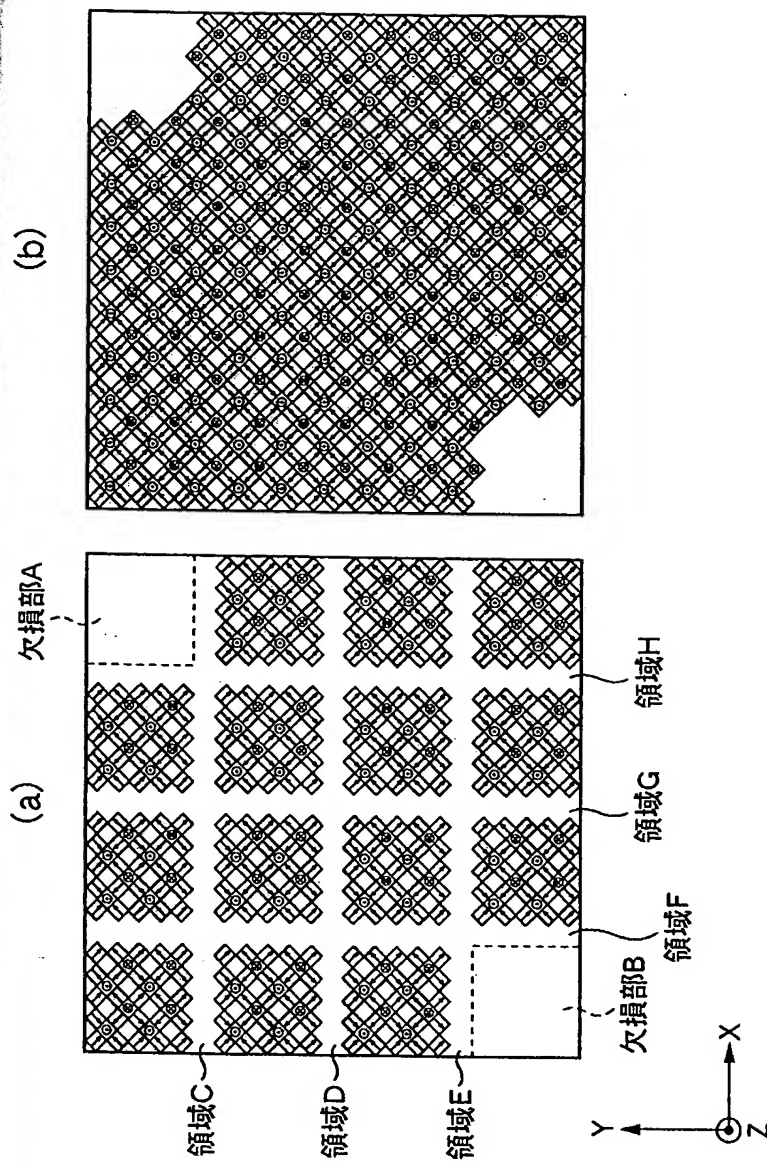
図 18]



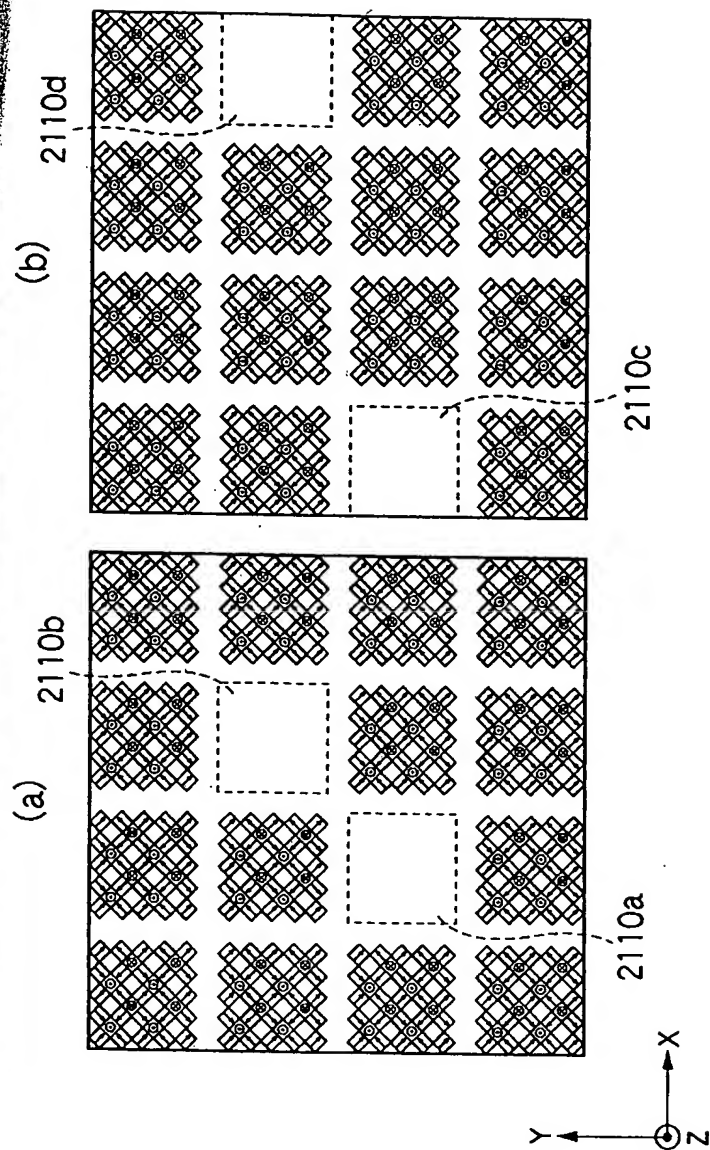
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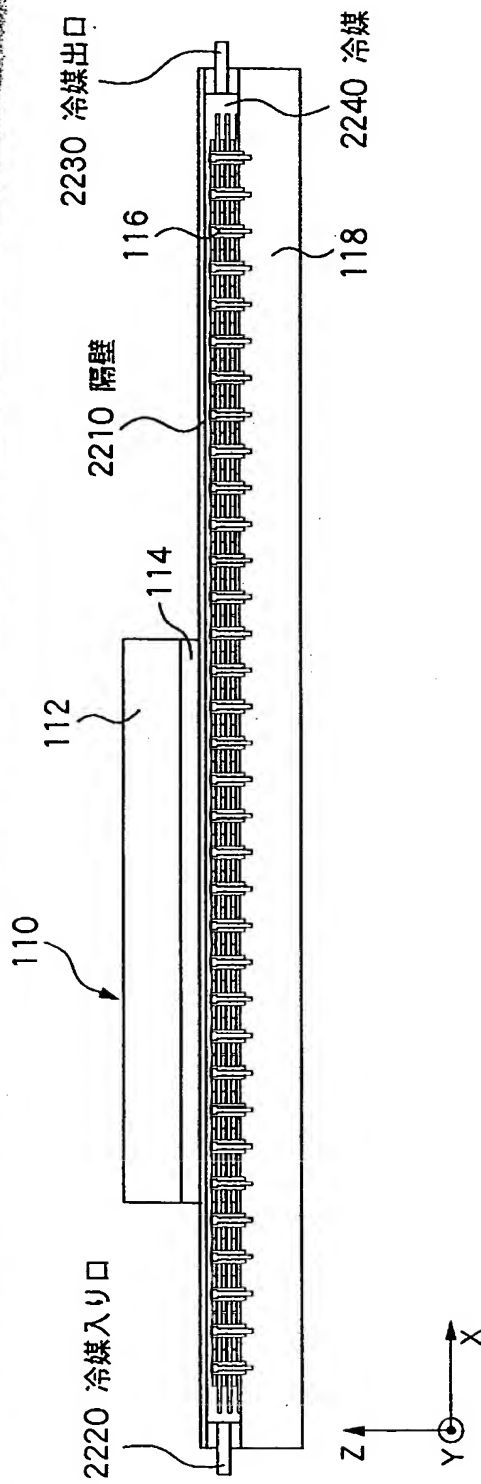
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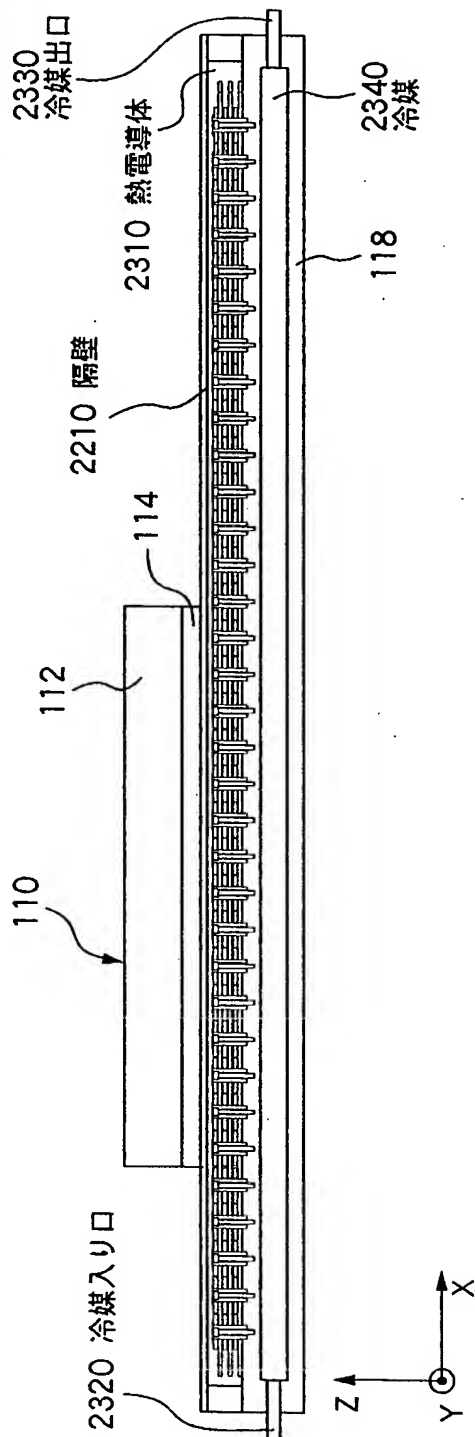
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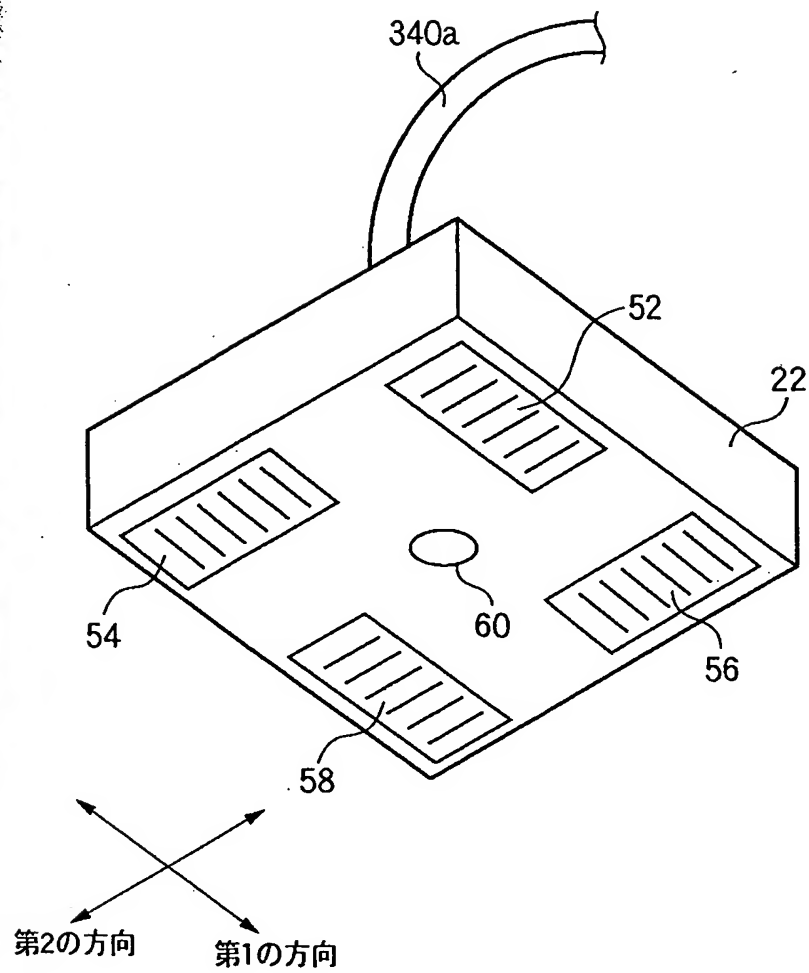
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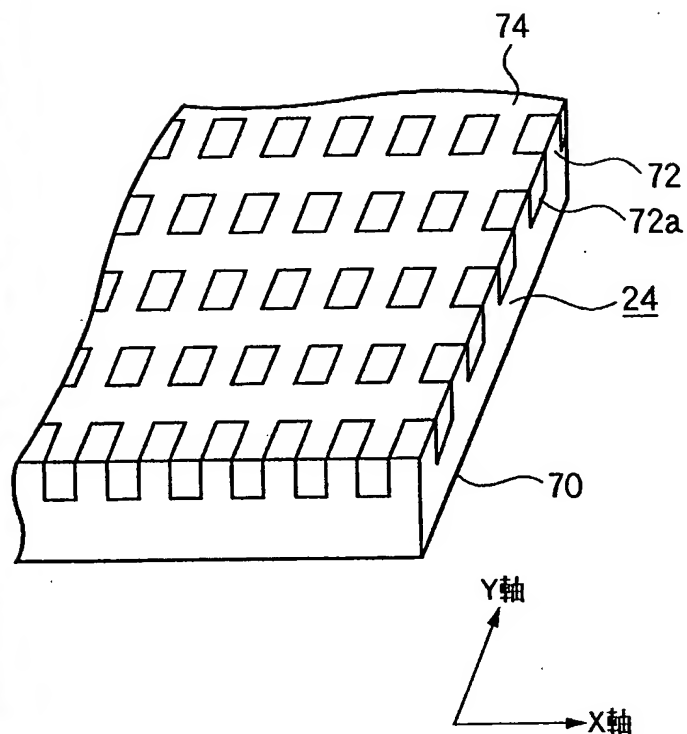
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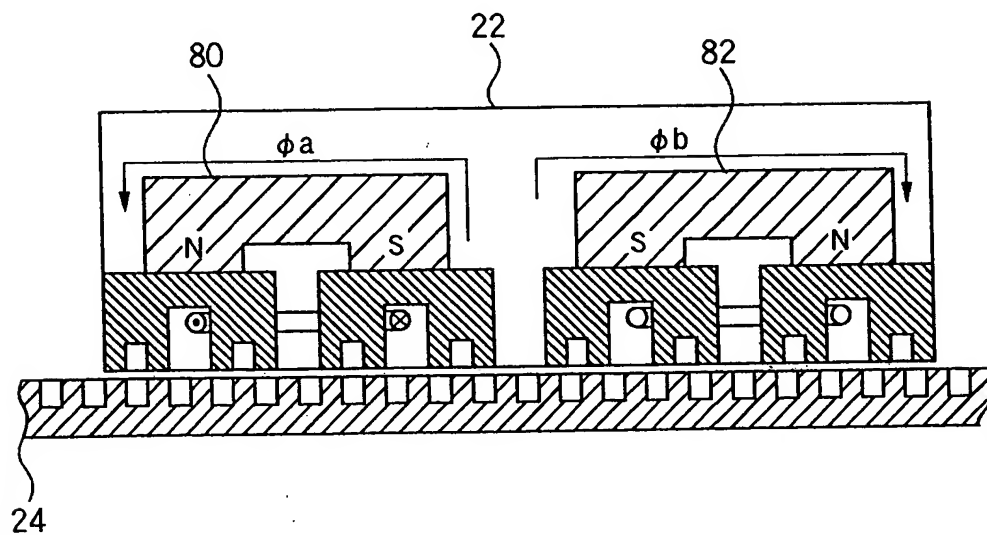
【図 24】



【図 25】



【図 26】



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